IN THE CLAIMS

Please amend the following claims which are pending in the present application:

1 – 15 (Canceled)

16. (Original) A method comprising:

forming a gate and a pair of sidewall spacers on either side of the gate above a single-crystal silicon substrate having a vertical [100] crystal plane, a horizontal [110] crystal plane, and a diagonal [111] crystal plane;

etching a recess in the single-crystal silicon substrate along the vertical [100] crystal plane with an anisotropic dry plasma etch;

implanting silicon into the bottom of the recess to form an amorphous etch stop;

etching the recess along the diagonal [111] crystal plane with an anisotropic wet etch having a pH of at least approximately 10 and no oxidizer; and

filling the recess with an electronically doped silicon germanium material to form a source/drain region.

17. (Original) The method of claim 16, further comprising a source/drain tip implant region under the sidewall spacers.

18. (Original) The method of claim 16, further comprising a shallow trench isolation region comprising an oxide and wherein the anisotropic wet etch does not etch the shallow trench isolation region or a hardmask protecting the gate.

19. (Original) The method of claim 16, wherein filling the recess with an electronically doped silicon germanium material forms an epitaxial source/drain tip extension region underneath the gate.

Claims 20 – 27 (Canceled)

28. (Original) A transistor, comprising:

a crystalline semiconductor substrate having a plurality of vertical [100] crystal planes, a plurality of horizontal [110] crystal planes, and a plurality of diagonal [111] crystal planes;

a gate electrode formed above the crystalline semiconductor substrate;

a pair of sidewall spacers, one on each side of the gate electrode; and

a pair of source/drain regions, one source/drain region under each of the sidewall spacers and wherein the source/drain regions are defined by the bottom of the spacers and by the diagonal [111] crystal planes.

29. (Original) The structure of claim 28, wherein the pair of source/drain regions extend beneath the pair of sidewall spacers by a distance of up to the width of one of the pair of sidewall spacers.

30. (Original) The structure of claim 28, wherein the pair of source/drain regions extend under the gate electrode by a distance in the approximate range of 10% and 20% of the width of the gate electrode.

Claim Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 1, 4, 5, 10-15, and 20-22 under 35 USC §103(a) as unpatentable over Gonzalez et al. (U.S. Patent No. 6,784,076) in view of Yasuda et al. (U.S. Patent No. 6,060,403). The Examiner has rejected claims 7, 9, 23-24 and 26-27 under 35 USC §103(a) as unpatentable over Gonzalez et al. (U.S. Patent No. 6,784,076) in view of Yasuda et al. (U.S. Patent No. 6,060,403) as applied to claims 1, 4, 5, 10-15, 20-22 and further in view of Kinugawa (U.S. Patent No. 4,857,986). Claims 1, 4, 5, 7-24 and 26-30 have been canceled.

The Examiner has allowed claims 16-19 and 28-30. The Applicant thanks the Examiner for the allowance of these claims.